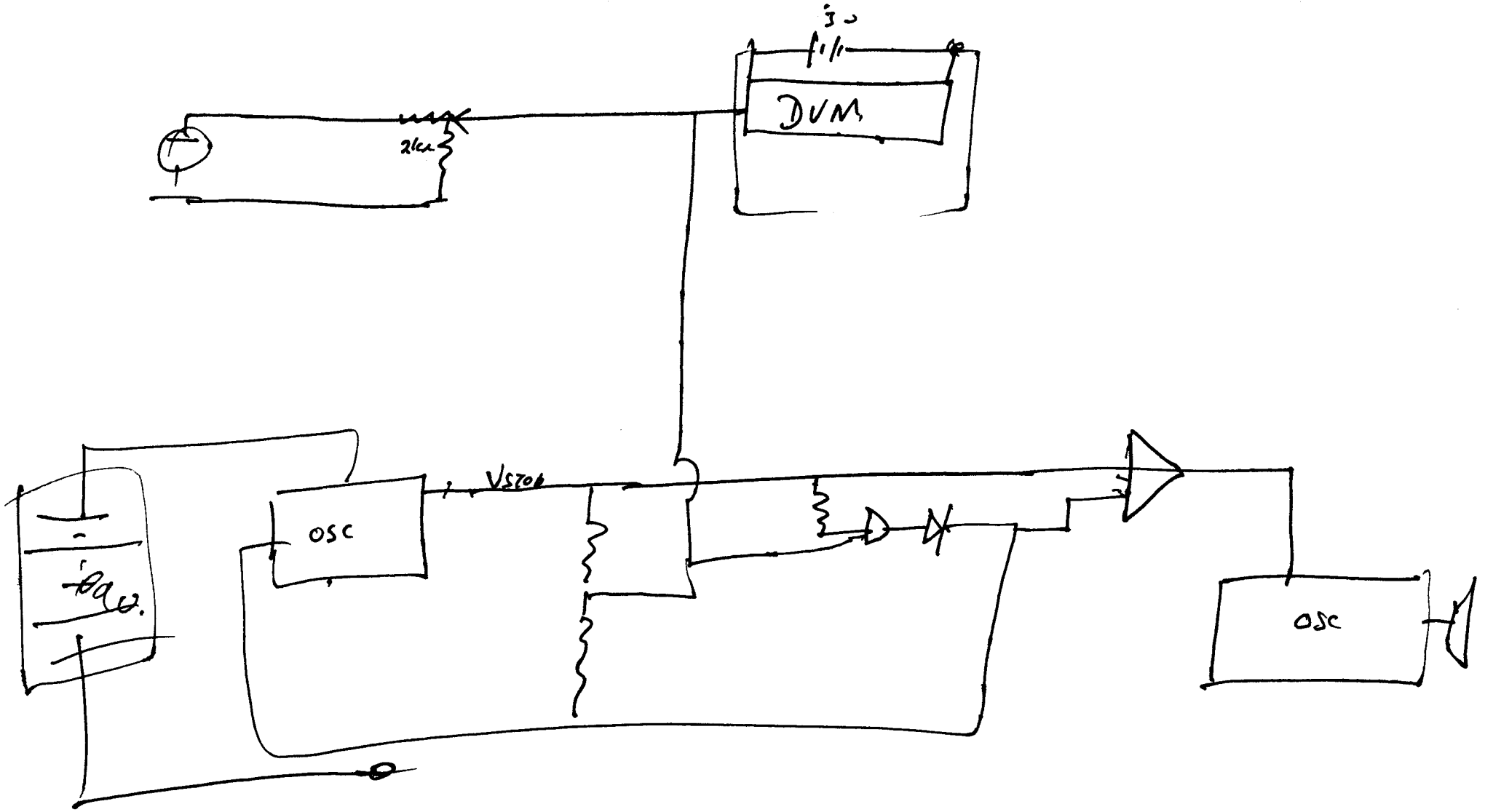
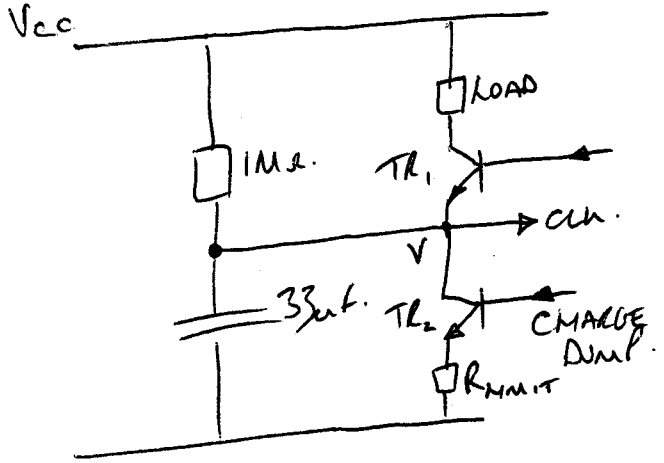


May 2020

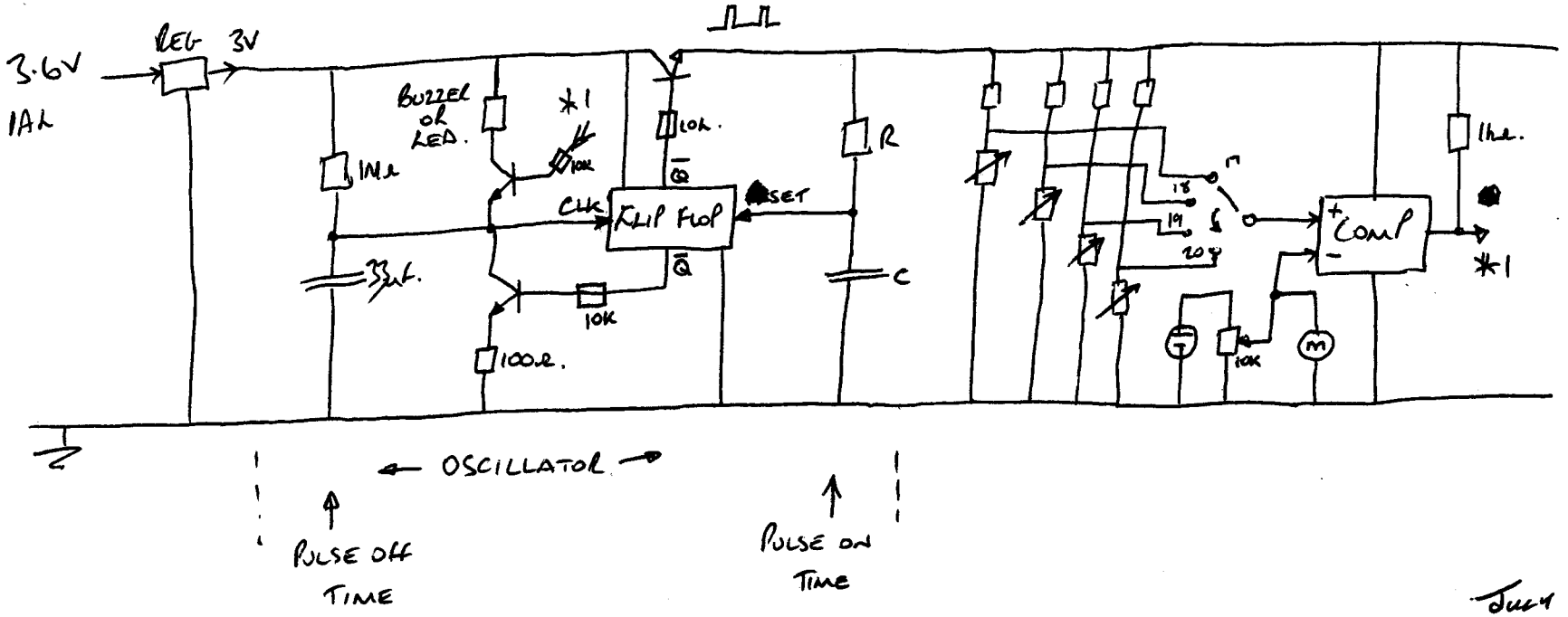


If LOAD = R_{LIMIT}, then $I_{C1} = I_{E1} \& I_{C2} = I_{E2}$ ∴ V≅ ½Vcc.

If LOAD ≫ R_{LIMIT}, then V ≫ GND

If R_{LIMIT} ≫ LOAD, then V ≫ Vcc

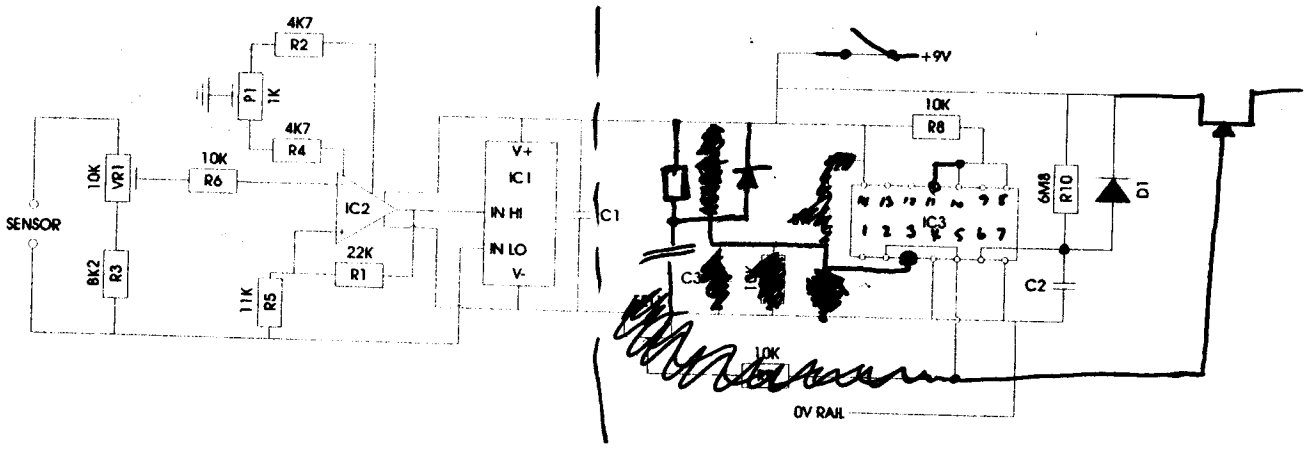
$CR = 1M\Omega \times 33\mu f = 33$secs.



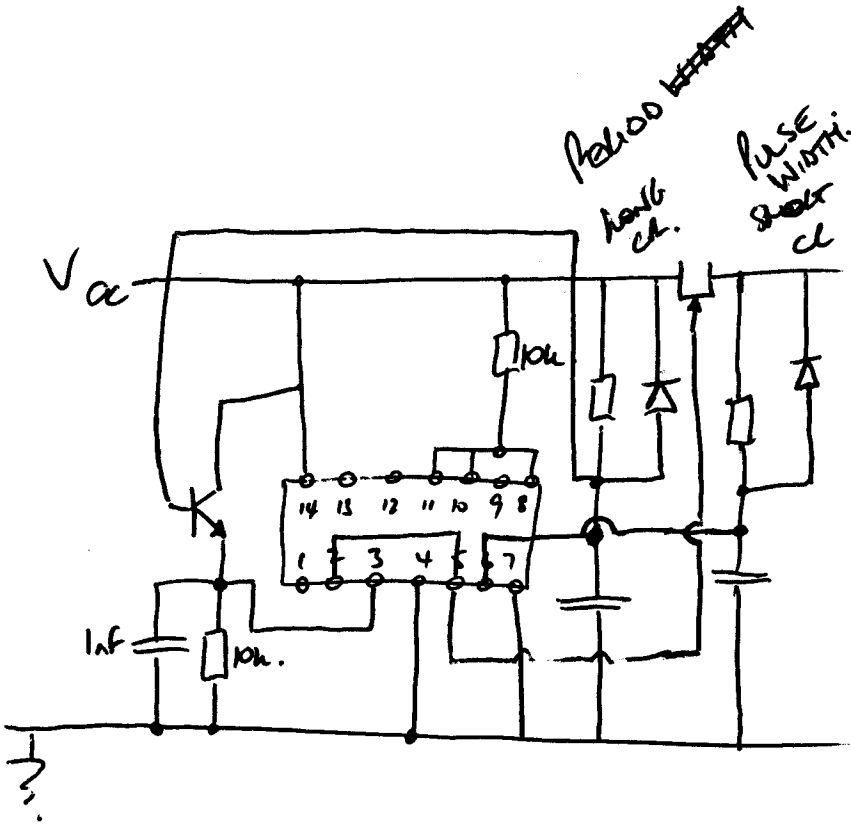
July 2020

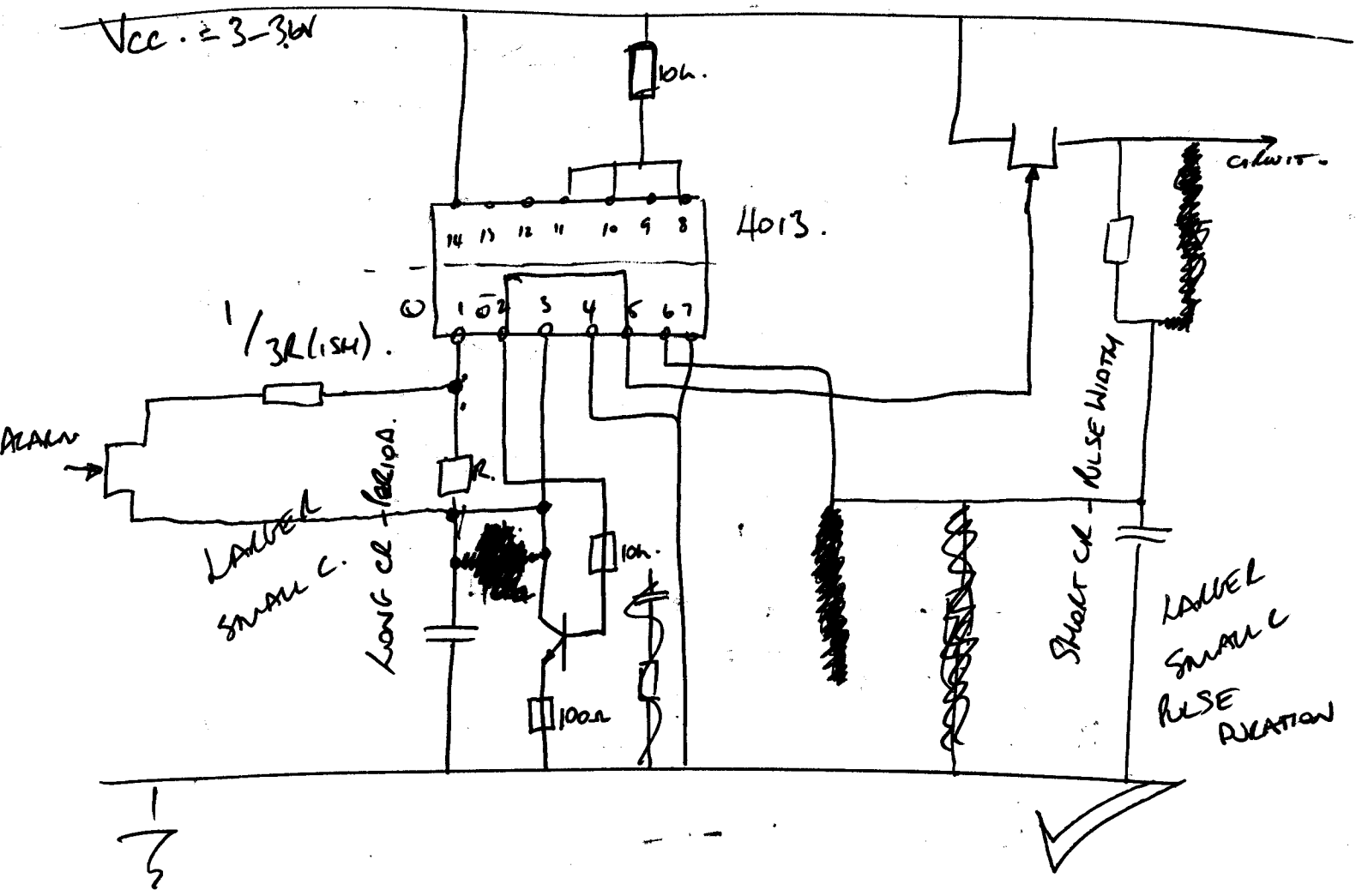
Circuit Design Considerations

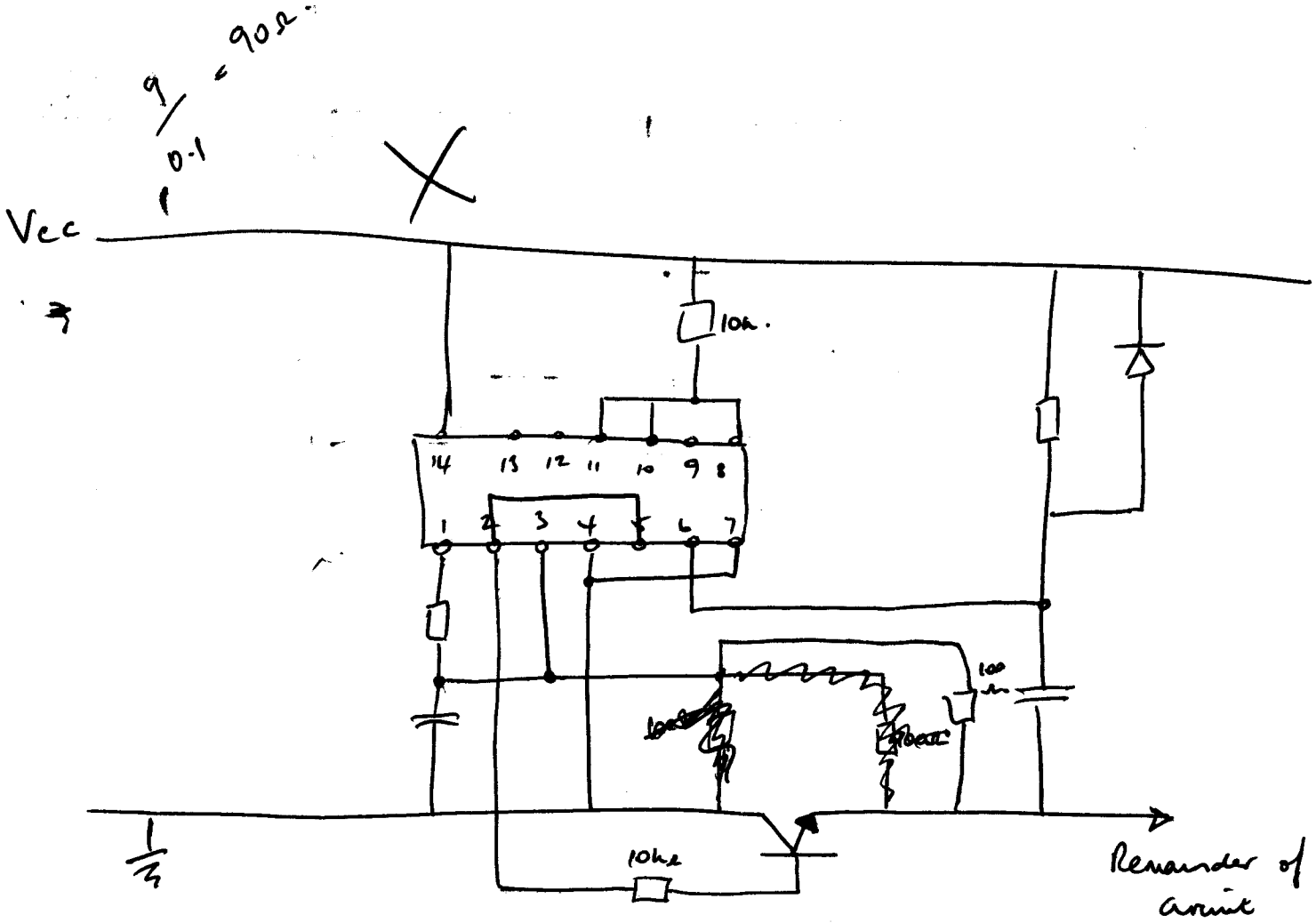
Circuit Schematic



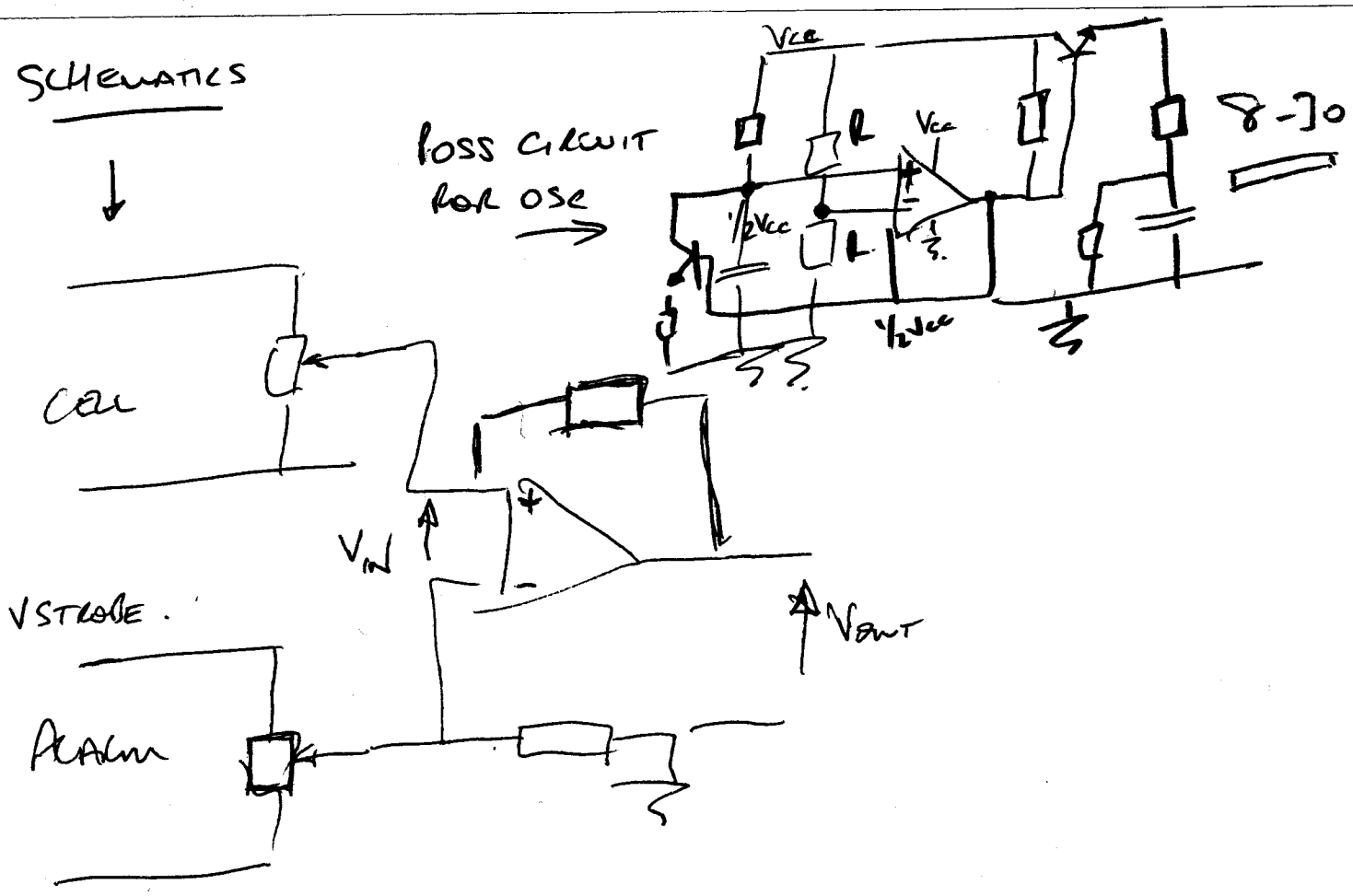
R1	22K	C1	10nF	IC1	DPM400
R2	4K7	C2	33*u*F	IC2	TL071CP
R3	8K2	C3	1nF	IC3	MC14013BCN
R4	4K7	VR1	10K		
R5	11K	P1	1K Multi		
R6	10K	FET1	VN10KM		
R8	10K	D1	1N4148		
R9	10K				
R10	6M8				
R11	10K				




Vcc. ≈ 3-3.6V
10k.
4013.
14 13 12 11 10 9 8
1 2 3 4 5 6 7
1/3R(ISH).
R.
10k.
100Ω
CIRCUIT.
PULSE WIDTH
LARGE C
SMALL C
LARGE
SMALL C
PULSE
DURATION


90Ω.
0.1
Vcc
10k.
14 13 12 11 10 9 8
1 2 3 4 5 6 7
100
10kΩ
Remainder of
circuit

SCHEMATICS



~~Job~~. STRS DURATION

Target: 43800 hrs. Cell cap 1AH. ⇒

Target average current draw = 22.83μA.

4.54μA @ 2.2s period / 50ms pulse + internal

3.13μA @ 3s period / 50ms pulse + internal

@ 20s period / 50ms pulse + internal

0.625μA.

1.1Ω.

238Ω.

344Ω