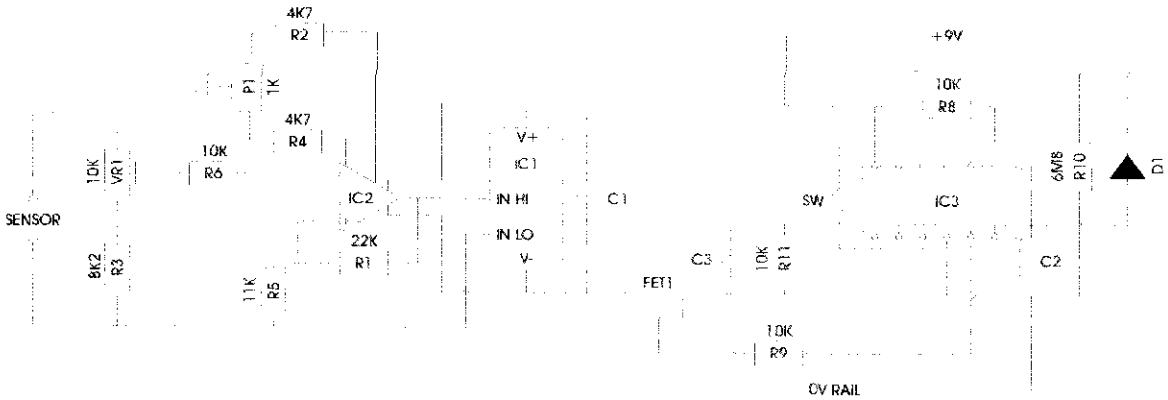
Circuit Design Considerations

Circuit Schematic



R1	22K	C1	10nF	IC1	DPM400
R2	4K7	C2	33*u*F	IC2	TL071CP
R3	8K2	C3	1nF	IC3	MC14013BCN
R4	4K7	VR1	10K		
R5	11K	P1	1K Multi		
R6	10K	FET1	VN10KM		
R8	10K	D1	1N4148		
R9	*10K*				
R10	6M8				
R11	10K				

Calculating the gain of the circuit

The fuel cell has an operational range of 7mV to 13Mv in air according to the specification of the manufacturer. Beyond these limits the performance of the fuel cell cannot be guaranteed, therefore it was necessary to design a circuit which would not allow a cell which is outside these limits to calibrate to 21%.
As the panel meter is being used in the circuit as a voltmeter it is necessary to have 21mV applied across it to give a reading of 21% in air. Since the minimum operational voltage of the fuel cell is 7mV then the amplifier must have a gain of 3 to obtain a reading of 21% when 7mV is applied to it. (fig.1)

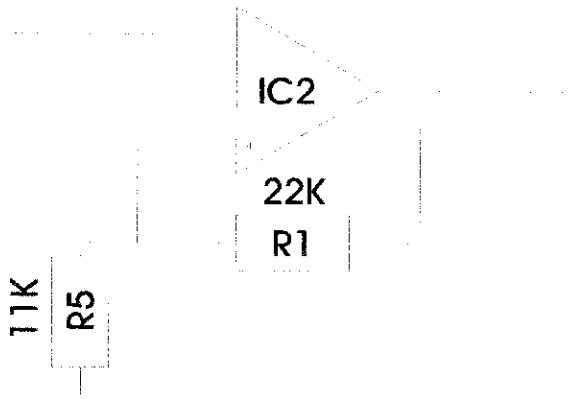
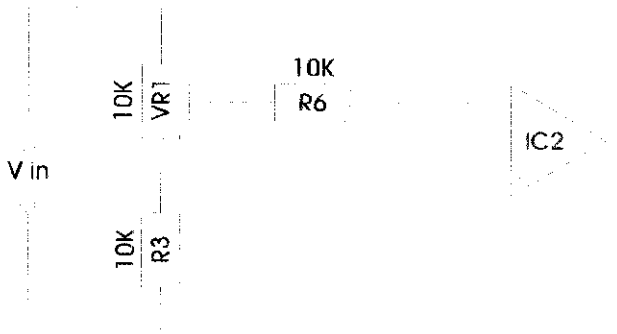


fig.1

Using $\frac{R1+R2}{R1}$ Gain = $\frac{11+22}{11}$ =3

If the gain of the amplifier is fixed at 3 then an input of 13mV, which is the maximum input we would want the circuit to allow to calibrate, would give a reading of 39%. It is therefore necessary to introduce a potential divider to the input to drop the voltage down to 7mV so the amplifier can multiply it by 3 to read 21%.

The initial circuit used in development used a 10K potentiometer and two 10K fixed resistors as a potential divider which could drop 13mV down to 6.5mV to provide a working prototype. It can be seen however that this is not ideal as it would allow input voltages as high as 14mV to read 21 on the panel meter which is beyond the specification of the cell. (fig.2)

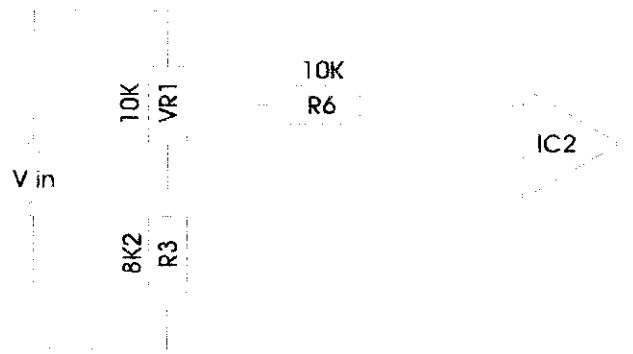


$$V\ in = 7mV \times \frac{10+10}{10}$$

$$V\ in = 14mV$$

fig.2

13mV divided by 7mV equals 1.82 therefore using a 10K pot in series with an 8K2 resistor will divide the input voltage by 1.82 which is very close to the ideal but will reject a cell marginally lower than 13mV rather than higher. (fig.3)



$$V\ in = 7mV \times \frac{10+8.2}{10}$$

$$V\ in = 12.74mV$$

fig.3

The table below shows the following:

The minimum voltage that will be present at the input to the op-amp, this is found by dividing the input voltage by 1.82 which will be the case when the potentiometer is turned down to its minimum value.

The maximum voltage at the op-amp which is the same as the input voltage, this is the case when the potentiometer is turned up to its maximum value.

The minimum and maximum percentage readings that will be seen on the display, this is found by multiplying the inputs to the op-amp by its gain of 3.

Voltage in; Min V at IC2	Max V at IC2	Min % reading on the LCD	Max % reading on the LCD
7mV	3.85mV	11.5%	21%
12.74mV	7.14mV	21.42%	39%

It can be seen from this table that the minimum input from the cell that can be calibrated to 21% is 7mV, and the maximum input that will calibrate is 13mV. Therefore the monitor will only allow the calibration of cells that are within the manufacturers specified limits.

Zero off-set adjustment

The op-amp IC2 has a null off-set between pins 1 and 5. The circuit incorporates a 1K trim pot in between two 4.7K resistors to allow the adjustment of the reading on the panel meter when no input voltage is present. During the calibration of the board this will be set to 00.0%. (fig.4)

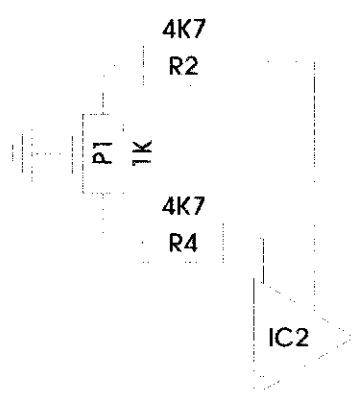


fig.4

Auto switch off timer

The rest of the circuit is concerned with the automatic switch off function. The delay time is controlled by R10 and C2. In order to de-bounce the on/off switch for more reliable operation the capacitor C3 was added to the circuit. (fig.5)

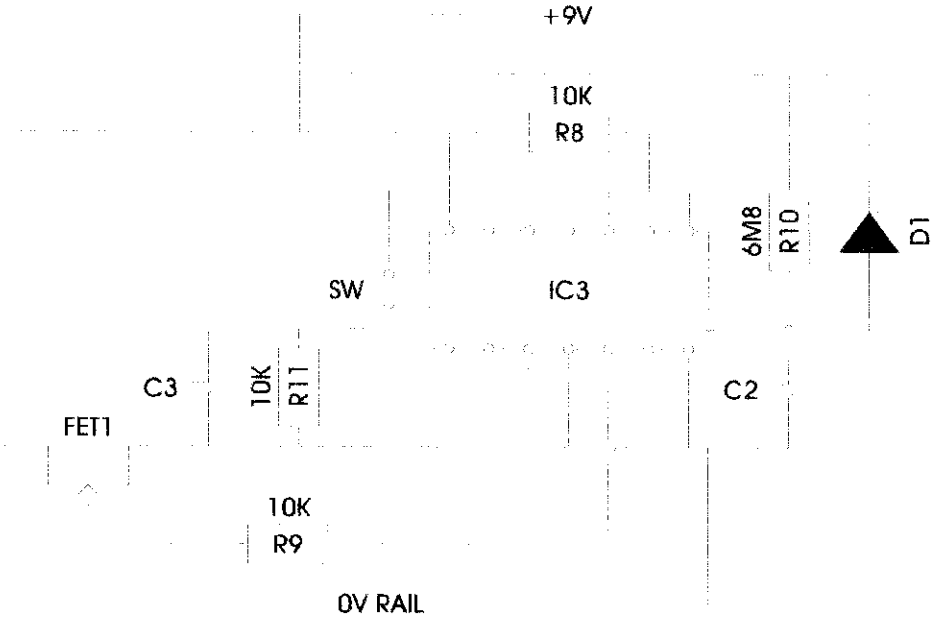


fig.5