APGAR V1.0 Circuit Operation.

Note: Design calculations are detailed in the "Hardware Design Detail" document.

Power supply.

The power requirements were:

To operate from "AA" size batteries,
To operate for a minimum of 12 months before a battery change is necessary,
To achieve a very low power dissipation design.

A high efficiency step-down switch-mode design was chosen to fulfil these requirements.

The controller used was an LTC1877 step-down converter in a standard design.
An input voltage range of 3.4V – 6.4V, from 4 off "AA" batteries, is converted to an output of 3.35V. This output voltage was chosen because of the tolerances in the ST7FLITE15 processor's Low Voltage Detect (LVD) Low Threshold specification – a maximum of 3.15V. The LVD circuit is used to reset the ST7 processor at power-up. So, to achieve minimum power dissipation, 3.35V was chosen for the V_{DD} supply. A "PP3" battery solution was considered but dropped due to the insufficient capacity of the PP3 battery.

High capacity ceramic capacitors were used for C2 and C4 in preference to tantalum or other electrolytic types, as their technical performance is better.

Processor and peripheral circuitry.

The processor is an ST7FLITE15, a twenty-pin device.

Power supply input.

The V_{DD} and V_{SS} pins are decoupled by a 0.1uF ceramic capacitor to provide noise and ESD pulse filtering. Bulk capacitance is provided by C2 in the power supply, which is mounted very close to the processor's power supply input pins on the PCB.

Oscillator.

The oscillator is a 32.768kHz crystal type chosen for accuracy and stability. C7 and C8 form the load for the crystal. The processor's internal 700kHz (at V_{DD}=3V) RC oscillator is not used in this design because of its poor stability and relatively high power consumption. Because of its higher frequency, it would also radiate more RF interference than the 32.768kHz oscillator will do.

A/D functionality and accuracy check.

The circuit IC3 and R5 is used to check the functionality and accuracy of the analogue-to-digital (A/D) converter. IC3 is a 1.22V voltage reference. It is fed from processor pin PB5 via R5. The reference voltage generated is monitored by

processor pin PB4 – the AIN4 A/D input. When the circuit is not in use, all three processor pins (PB4, PB5 and PB6) are at V_{SS} level to minimise power dissipation. In use, PB6 is kept at V_{SS} whilst PB5 is raised to approximately V_{DD}. The reference voltage at PB4 is converted to digital form and compared to a target window of digital values. If the result is within this window then the A/D converter is considered functional and accurate, otherwise an error is reported. This test is not foolproof. It does not use the A/D input which actually monitors the battery voltage, so that input could be faulty and not be detected.

Battery monitoring.

A battery monitoring circuit comprising R3, R4, C9 and D3 feeds the AIN0 input to the processor and the internal analogue-to-digital converter. R3 and R4 form a potential divider such that when the batteries are new, the 6.4V battery voltage is brought within the A/D input range – less than V_{DD}. C9 provides noise filtering. D3 protects the processor AIN0 input from damage in case R4 goes open circuit by clamping the input to one (Schottky) diode voltage drop above V_{DD}.

The battery voltage is checked once a day and compared to a 4V threshold. If the voltage is below 4V, then a "Lo BAtt" message is displayed on the LCD.

Sounder.

A piezo-electric sounder is attached to processor pin PA4, the PWM2 output pin. The pulse width modulator controls the frequency and amplitude of the APGAR and key-press beeps. Diode D2 protects the processor pin from any voltage spikes produced by the sounder.

Keypad inputs.

Processor pins PA3 (Start), PA2 (Freeze) and PA1 (Reset) are the inputs from the press-to-make membrane keypad switches. Each switch connects an input to V_{SS} when made. Each pin has an internal pull-up resistor, so an external resistor is not required. Resistors R14, R15 and R16 provide some protection against any ESD pulses induced into the membrane's keypads. The membrane keypads connect to the PCB via CN1.

Programming and debugging inputs.

A six-way connector, CN2, provides the programming and debugging interface to the design. The pin functions are:

CN2/1	V_{SS}
CN2/2	V_{DD}
CN2/3	Processor reset. A pull-up resistor, R17, enhances noise immunity.
CN2/4	ICCCLK. This pin provides the programming/debug clock to the processor. A pull-up resistor, R9, provides enhanced noise immunity.
CN2/5	ICCDATA. This pin provides programming/debug data. A pull-up resistor, R8, provides enhanced noise immunity.
CN2/6	OSC1. This is the CPU's external clock input, if needed.