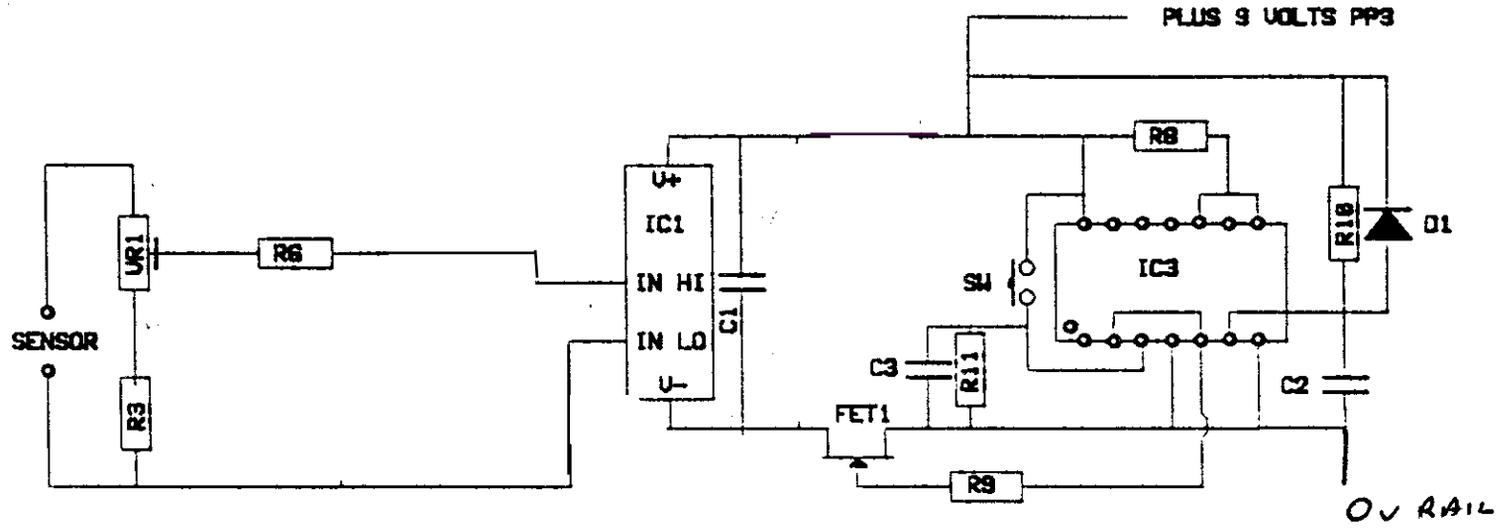


C1 10NF

C2 33MFD IC1 OPM400

R3 8K2 C3 SEE NOTE

R4 4.7K VR1 10K IC3 MC14013BCP

R6 10K

DISP OPM400

FET1 VN10KM

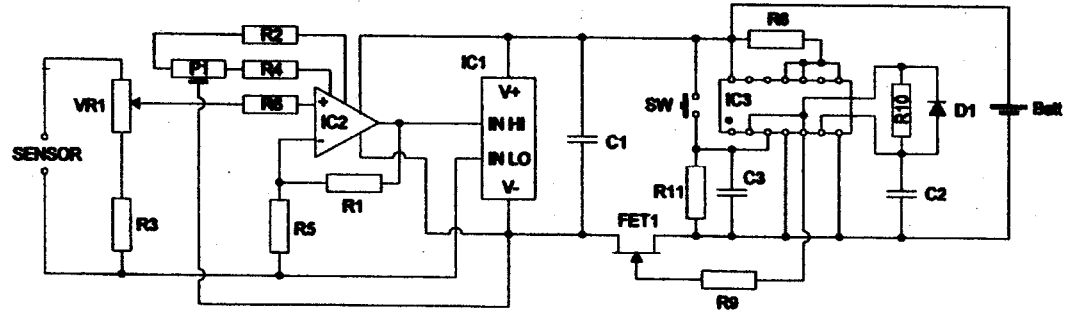
R8 10K

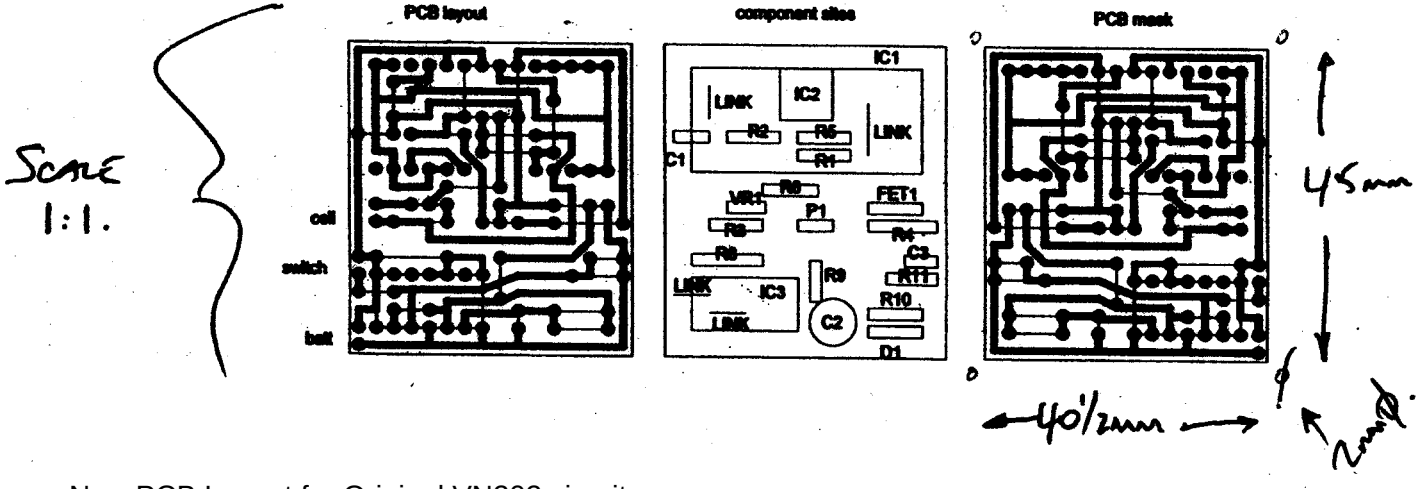
R9 10K D1 1N418

R10 6M8

R11 10K

COMPANY VANDAGRAPH	DRAWING
MODEL	DRAWING NUMBER
DATE 1 AUG 1984	ENGINEER MR T MELLIN

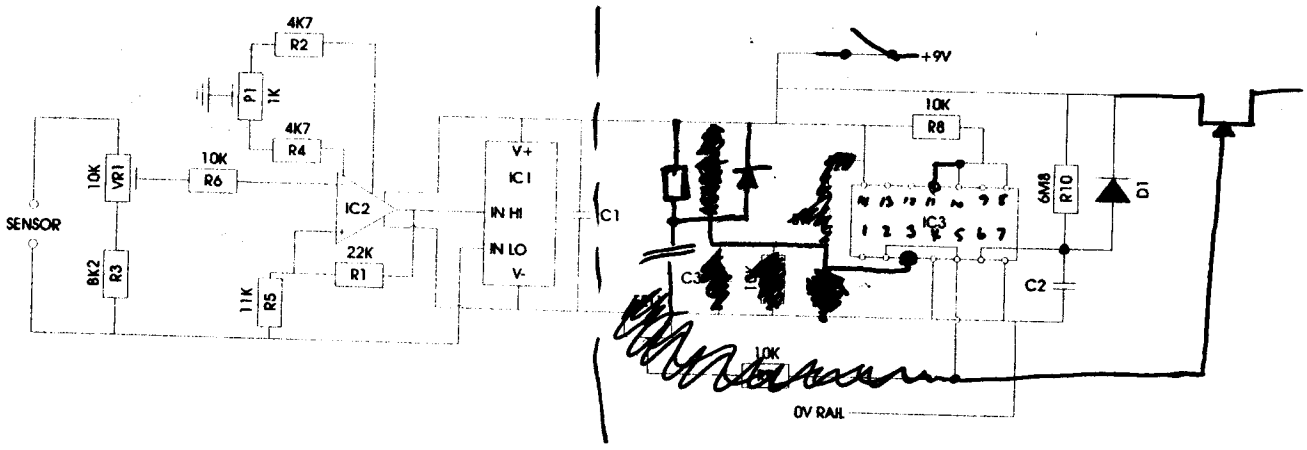




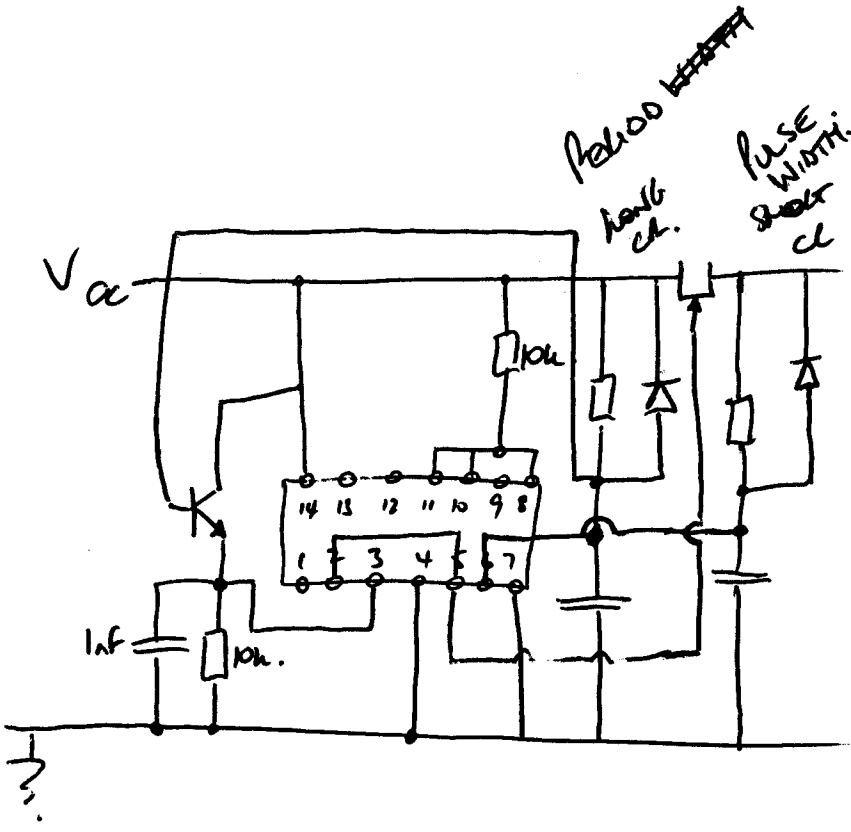
New PCB Layout for Original VN202 circuit

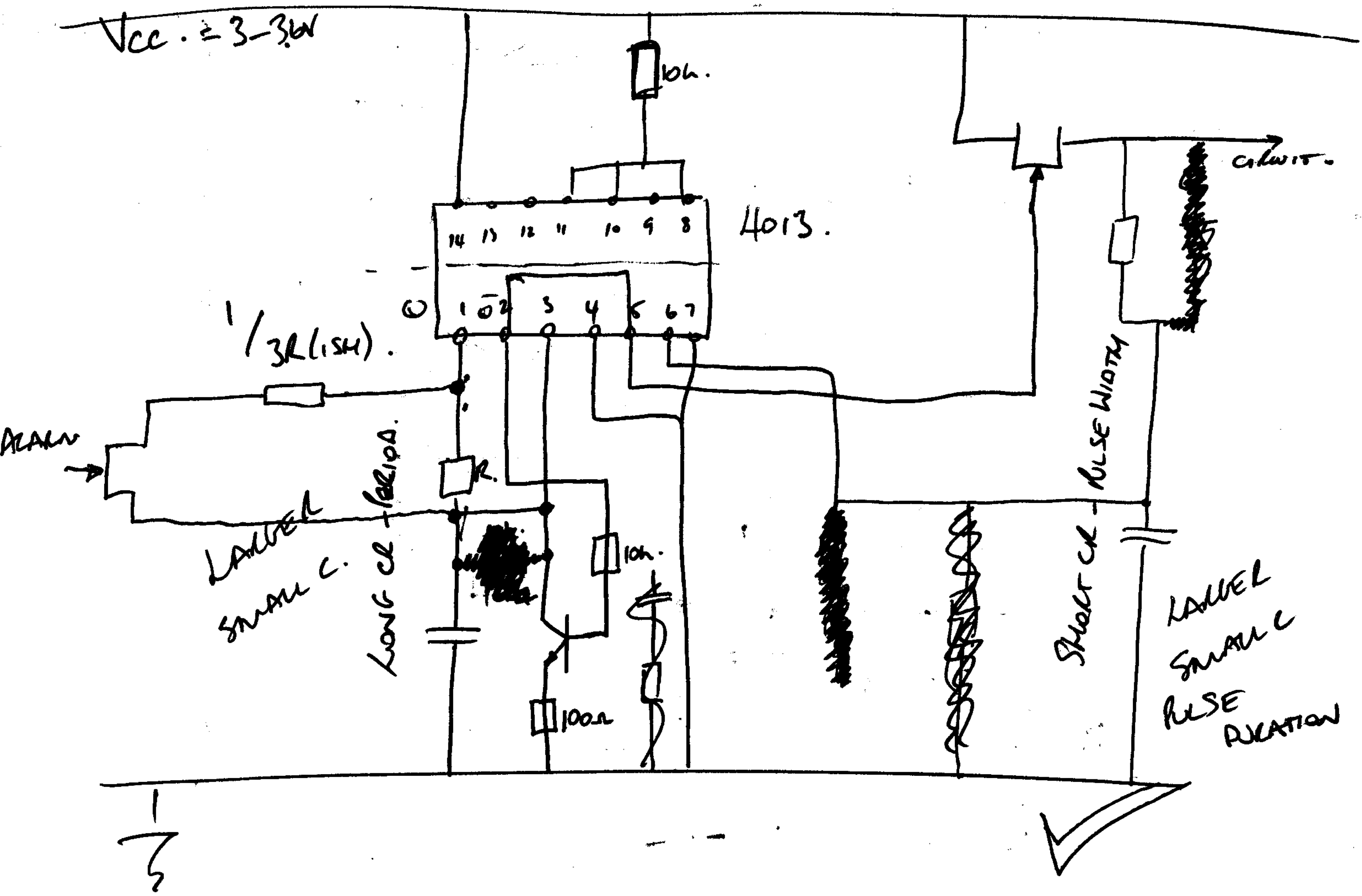
Circuit Design Considerations

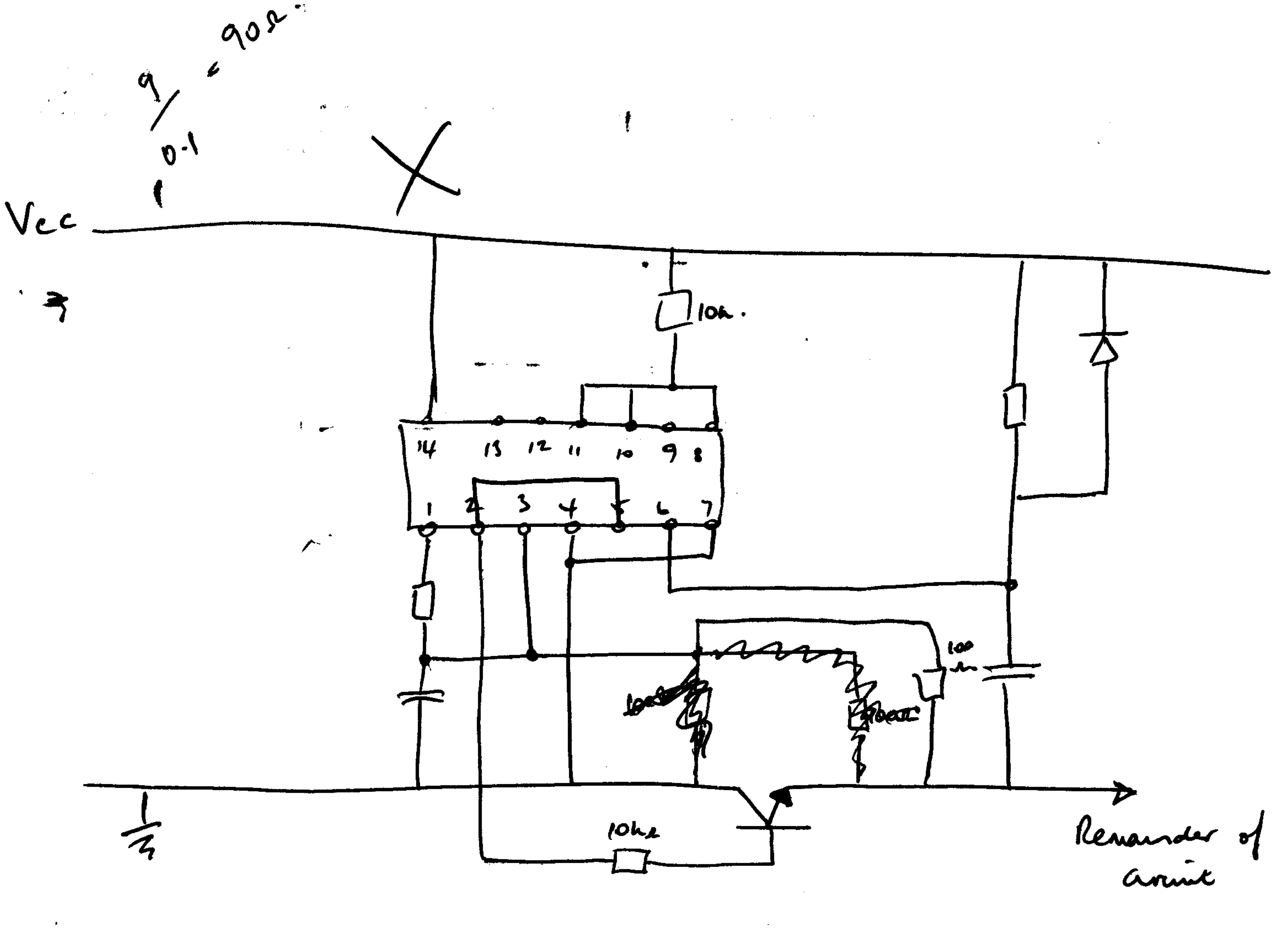
Circuit Schematic



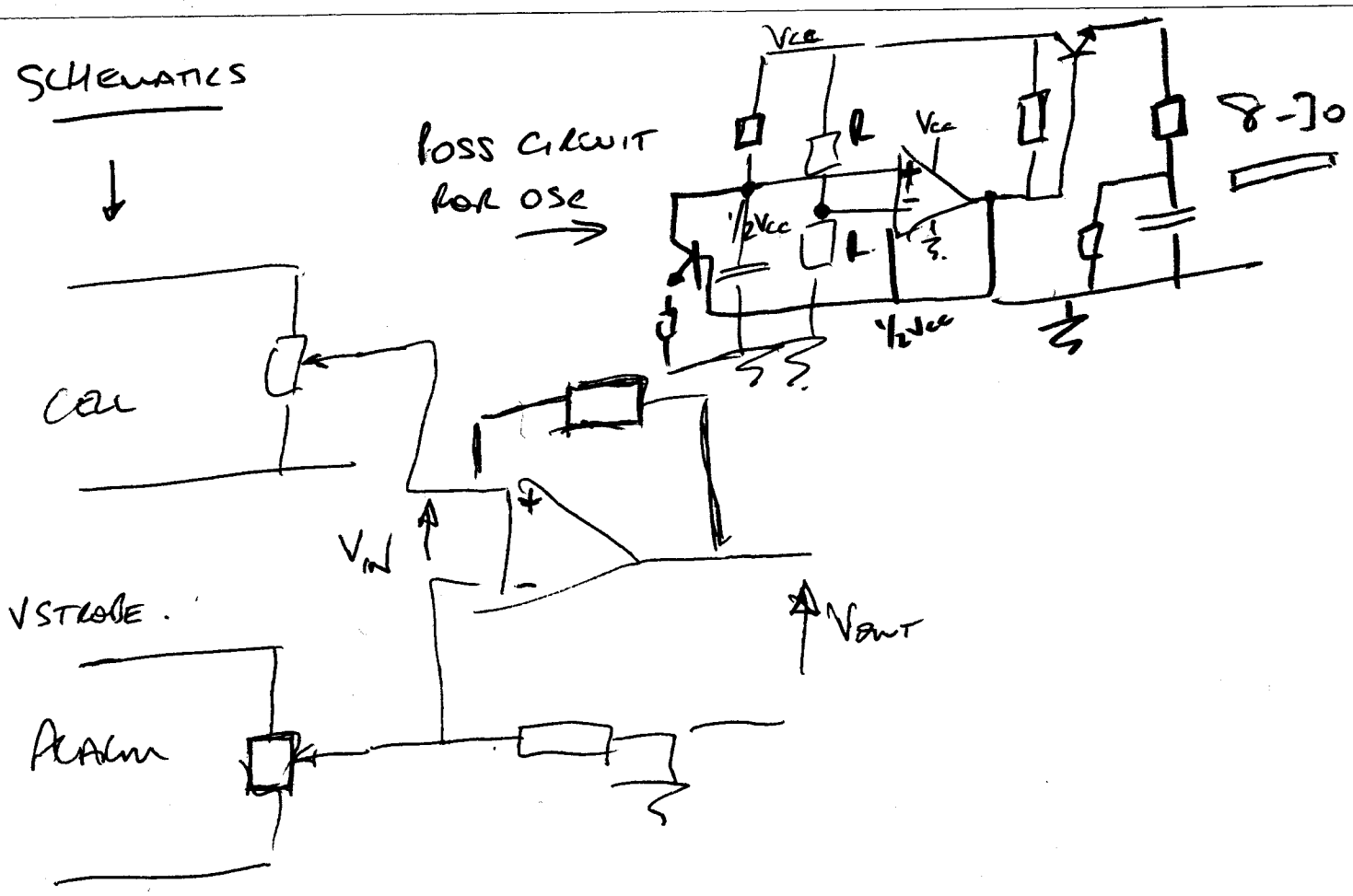
R1	22K	C1	10nF	IC1	DPM400
R2	4K7	C2	33*u*F	IC2	TL071CP
R3	8K2	C3	1nF	IC3	MC14013BCN
R4	4K7	VR1	10K		
R5	11K	P1	1K Multi		
R6	10K	FET1	VN10KM		
R8	10K	D1	1N4148		
R9	10K				
R10	6M8				
R11	10K				




Vcc. = 3–3.6V
10k.
4013.
1/3R(ish).
ALARM
R.
LARGER
SMALL C.
LONG CR - PERIOD
10k.
100Ω
SHORT CR - PULSE WIDTH
LARGER
SMALL C
PULSE
DURATION


9/0.1 = 90Ω
Vcc
10k.
10kΩ
Remainder of
circuit

SCHEMATICS



~~Job~~. STRS DURATION

Target: 43800 hrs. Cell cap 1AH. ⇒

Target average current draw = 22.83μA.

4.54μA @ 2.2s period / 50ms pulse + internal

3.13μA @ 3s period / 50ms pulse + internal

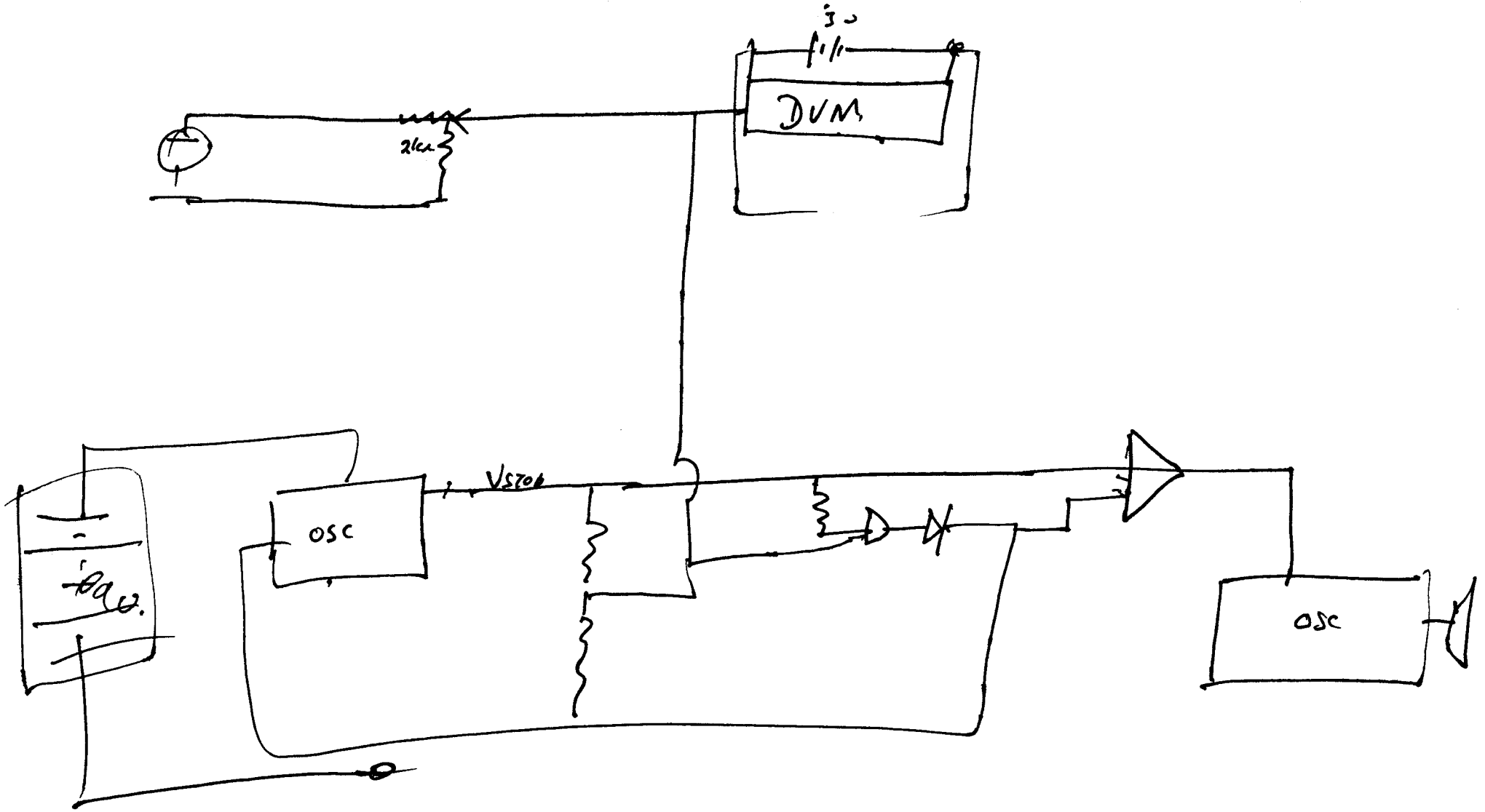
@ 20s period / 50ms pulse + internal

0.625μA.

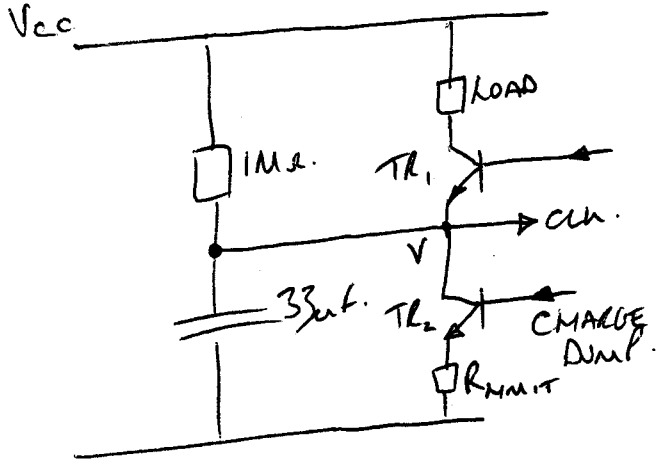
1.1Ω.

238Ω.

344Ω



May 2020

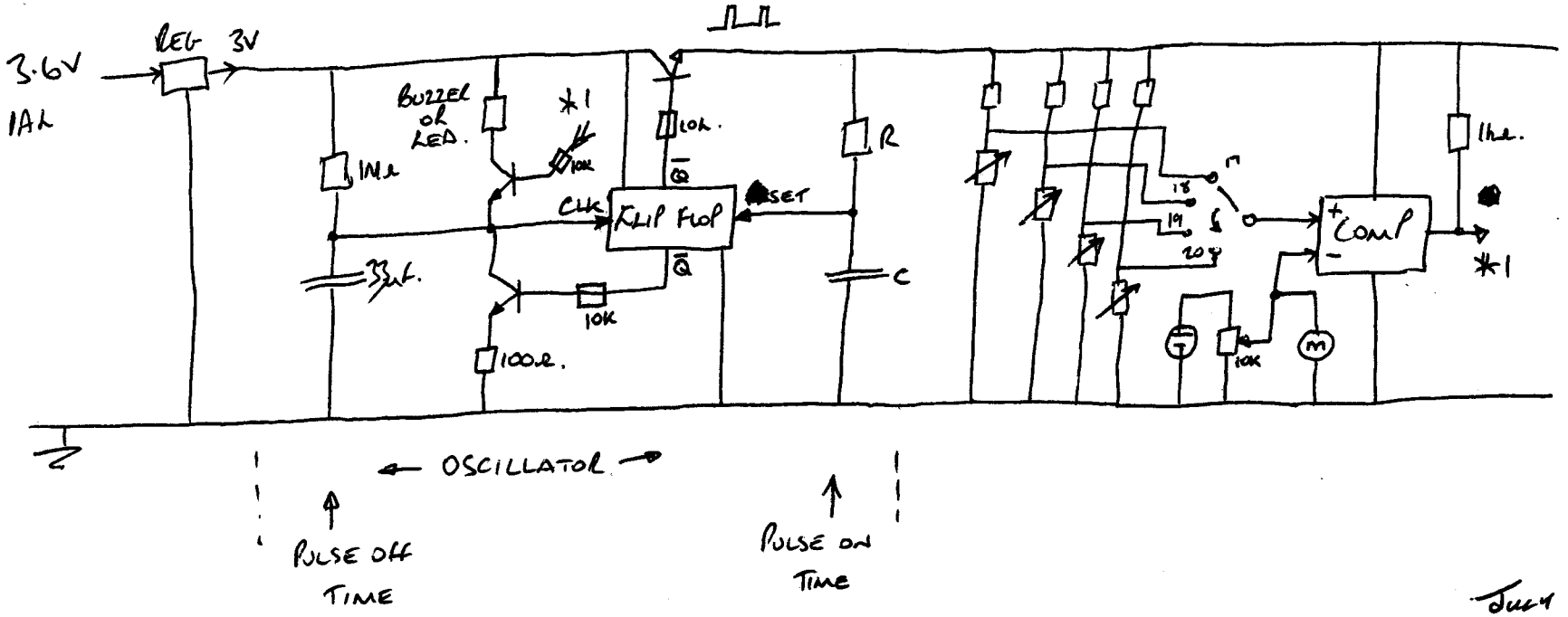


If LOAD = R_{LIMIT}, then $I_{C1} = I_{E1} \& I_{C2} = I_{E2}$ ∴ V≅ ½Vcc.

If LOAD ≫ R_{LIMIT}, then V ≫ GND

If R_{LIMIT} ≫ LOAD, then V ≫ Vcc

$CR = 1M\Omega \times 33\mu f = 33$secs.



July 2020