APGAR V1.0 Hardware Design Detail.

Power supply.

Battery type.

"AA" style batteries were chosen for their large capacity and worldwide availability.

Battery life.

Assumptions:

1 The timer will never be turned OFF – there will always be some LCD activity.

2 The timer will be used twice a day, 365 days a year.

3 The sounder will operate at the 1, 5 and 10-minute points with 1, 2 and 3 pulses each of 1 second duration.

4 The battery will be monitored once a day.

Calculation:

Number of hours in a year:	24 x 365	8760	
ST7FLITE15			
CPU (Estimated):			
Wait mode @ 32.768kHz	200 µA		
Run mode @ 32.768kHz	200 µA		
Consumption:	200 µA x 8760	1752 mAh	(1)

LVD/AVD	245 µA		
	245 µA x 8760	2146 mAh	(2)
RC Oscillator (Not used)		0 mAh	
PLL (Not used)		0 mAh	
12-bit timer AT2	50 µA		
	(50 µA x 2(Use) x 6(Times) x 1(Second) / 3600(Hours)) x 365	0.06 mAh	(3)
SPI (Not used)		0 mAh	
ADC	1.2 mA		
ADC (Calibration check)	(1.2 mA x 1(Sample) x 0.9 mS(Conversion time) / 3600(Hours)) x 365	0.11 mAh	(4)
ADC (Battery check)	(1.2 mA x 1(Sample) x 0.9 mS(Conversion time) / 3600(Hours)) x 365	0.11 mAh	(5)
Flash Memory			
No Read/Write	100 µA		
	100 µA x 8760	876 mAh	(6)
Read	2.6 mA		
	(2.6 mA x 256(Instructions) x (4 / 16384)(Instruction cycles)) x 8760	1424 mAh	(7)
Ports (Leakage)	1 µA		
	1 µA x 15(Pins) x 8760	131 mAh	(8)

PCF8576C LCD Driver

Supply (Power-saving mode)	60 µA		
	60 µA x 8760	526 mAh	(9)

Sounder	2.5 mA ((2.5 mA x 2(Use) x 6(Times) x 1(Seconds)) / 3600(Hours)) x 365	3 mAh	(10)
I2C interface	2(Lines) x 3.35V / 2700 Ohms x 1/1000(Duration) x 3600(Hours) x 8760	78 mAh	(11)
Battery Potential Divider	10 µA 10 µA x 8760	88 mAh	(12)
LTC1877 Regulator (1-5 mA load)	15 µA 15 µA x 8760	131 mAh	(13)
	Total (1 – 13)	7155 mAh	

Battery capacity required: 7155 mAh

"AA" Battery capacity by manufacturer:

Varta 4106	2600 mAh
Duracell MN1500	2700 mAh
Energizer Ultra Alkaline	2850 mAh

Number of batteries required: 7155/2600 — 2.75 batteries

Switching regulator.

Battery voltage (max): 4 x “AA” = 4 x 1.6V = 6.4V
Battery voltage (min): 4 x 0.8V = 3.2V

$LVD_{RISE\ (MAX)}$: 3.15V
V_{DD}: 3.35V

V_{BAT754}: 260mV @ 1mA
For regulation: V_{IN} = 3.4V @ V_{BAT} = 3.7V

V_{TRIP}: 3.7V + 260mV => 4.0V

The power supply was designed with the Linear Technology Switcher CAD III design package. An LTC1877 high efficiency step-down converter was used. Various component value options were tried until the current optimised design was achieved.

One addition to the design was the inclusion of diode D1. This diode provides reverse battery connection protection, as the LTC1877 controller chip does not have this facility. A BAT754 Schottky diode was chosen for its very low forward voltage drop – enhanced by the very low current through it – about 1mA. Despite this, the diode decreases circuit efficiency by about 10%.

C2 (47uF) and C4 (22uF) are high capacity ceramic capacitors – this type has better performance characteristics than tantalum or other electrolytic capacitors.

Processor and peripheral circuitry.

Processor (IC2).

An ST7FLITE15 processor was chosen. This is a twenty-pin device in an SM DIL format. Its features are:

Flash program memory – ICP capability for development and upgradability
Low operating voltage
Low current consumption modes for high efficiency – long battery life
Low frequency crystal oscillator capability for RTC operation
On-board timers for RTC operation
On-board A/D for battery monitoring
On-board PWM for a sounder
Designed with ESD in mind
Low cost

Power supply input.

C5 is 0.1uF for ESD protection and power supply noise decoupling.
C2 (47uF), in the power supply, provides ESD and bulk capacitance. It is mounted very close to the processor's power supply input pins on the PCB.

32.768kHz Crystal Oscillator.

C-MAC 85SMX crystal:

Frequency tolerance: +/- 20ppm at 25°C.
Temperature stability: +/- 80ppm.

Load capacitance: 22pF.

At 25°C:

Frequency variation = +/- (32768 x 20) / 1,000,000 = +/- 0.655536 Hz

Maximum timing error after 60 minutes = +/- (0.655536 / 32768) x 3600 = +/- 0.072018 S

= +/- 72mS

A/D Functionality and accuracy check.

IC3 is a ZXRE125FFTA 1.22V voltage reference. It was chosen for its reasonable accuracy, low cost and SMD format.

R5 was calculated as:

$$(V_{PORT} - (V_{DD} - V_{OH}) - V_{REF}) / 20\mu A = (3.35V - 0.8V - 1.22V) / 20\mu A \Rightarrow 68k\Omega$$

Battery monitoring.

The circuit comprises R3, R4, C9 and D3.

R3 and R4 form a potential divider of the input voltage after the reverse battery protection diode, D1. The centre point of the divider is set so that it is less than V_{DD} (3.35V) but close to it – to get the greatest A/D converter span. R3 and R4 were calculated as:

A/D leakage current:	1 µA
Divider current:	10 µA
V_{BAT754}:	260 mV @ 1 mA
V_{IN}:	$V_{BATT} - V_{BAT754}$ = 6.4V – 260 mV = 6.14V
R_{TOTAL}:	6.14V / 10 µA = 614 kΩ
R4:	(3.35V / 6.14V) x 614 kΩ => 330 kΩ
R3	614 kΩ- 330 kΩ => 287 kΩ

Capacitor C9 provides noise decoupling.
Diode D3 protects the AIN0 processor input pin against over voltage if R4 goes open circuit. It does this by clamping the input to one (Schottky) diode voltage drop above V_{DD}.

Sounder.

The SFM-1740 sounder was chosen because of its very low current consumption (less than 2.5 mA), its SMD format and low cost.
Diode D2 protects the processor pin against any voltage spikes generated by the sounder.

Keypad inputs.

Resistors R14, R15 and R16 provide some protection against any ESD pulses induced into the membrane keypad. Their value is standard for the application.

Programming and debugging inputs.

Resistors R8 and R9 are standard value pull-ups to enhance the noise immunity of the processor inputs.
Resistor R17 is a standard value for the reset pin pull-up. It supplements the processor's own internal pull-up resistor to enhance the pin's noise immunity.

I2C communications interface.

Resistors R6 and R7 are standard value pull-up resistors for I2C bus applications.

Spare processor pins.

R10 and R11 are standard value pull-up/down resistors for unused processor pins. Unused pins must not be left floating or connected directly to V_{DD} or V_{SS} in case of EMC/ESD interference.

LCD controller (IC4).

Capacitor C6 is 0.1uF for ESD protection and power supply noise decoupling.

The I2C-bus sub address (A0 – A2) is set to zero.

The I2C-bus slave address bit “0” (SA0) is set to zero.

As the LCD controller’s internal oscillator is used, pin “OSC” is grounded.

The LCD supply voltage bottom end is set to zero by grounding the pin $V_{LCD.}$

The pin “/SYNC” is not used and is left open-circuit.

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