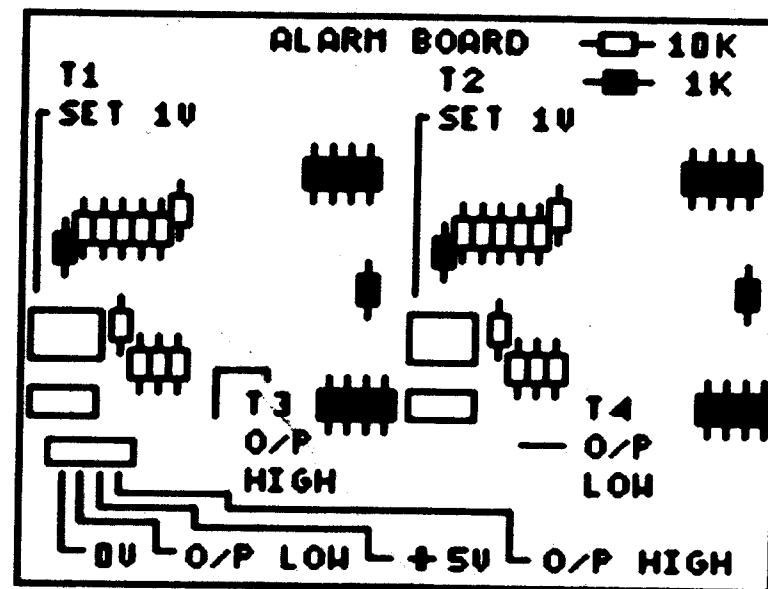
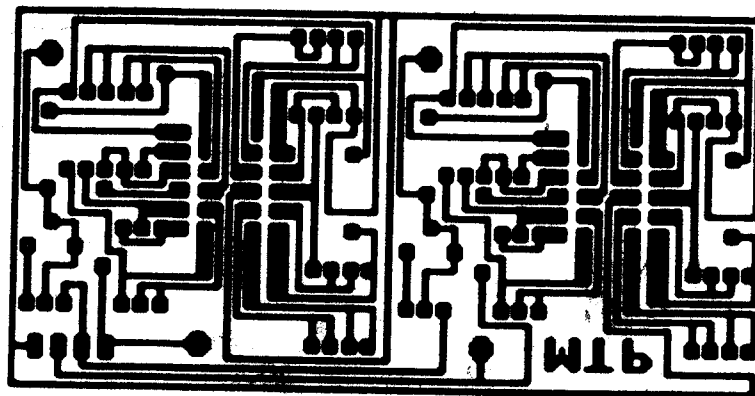


FINAL



500

100k
90k

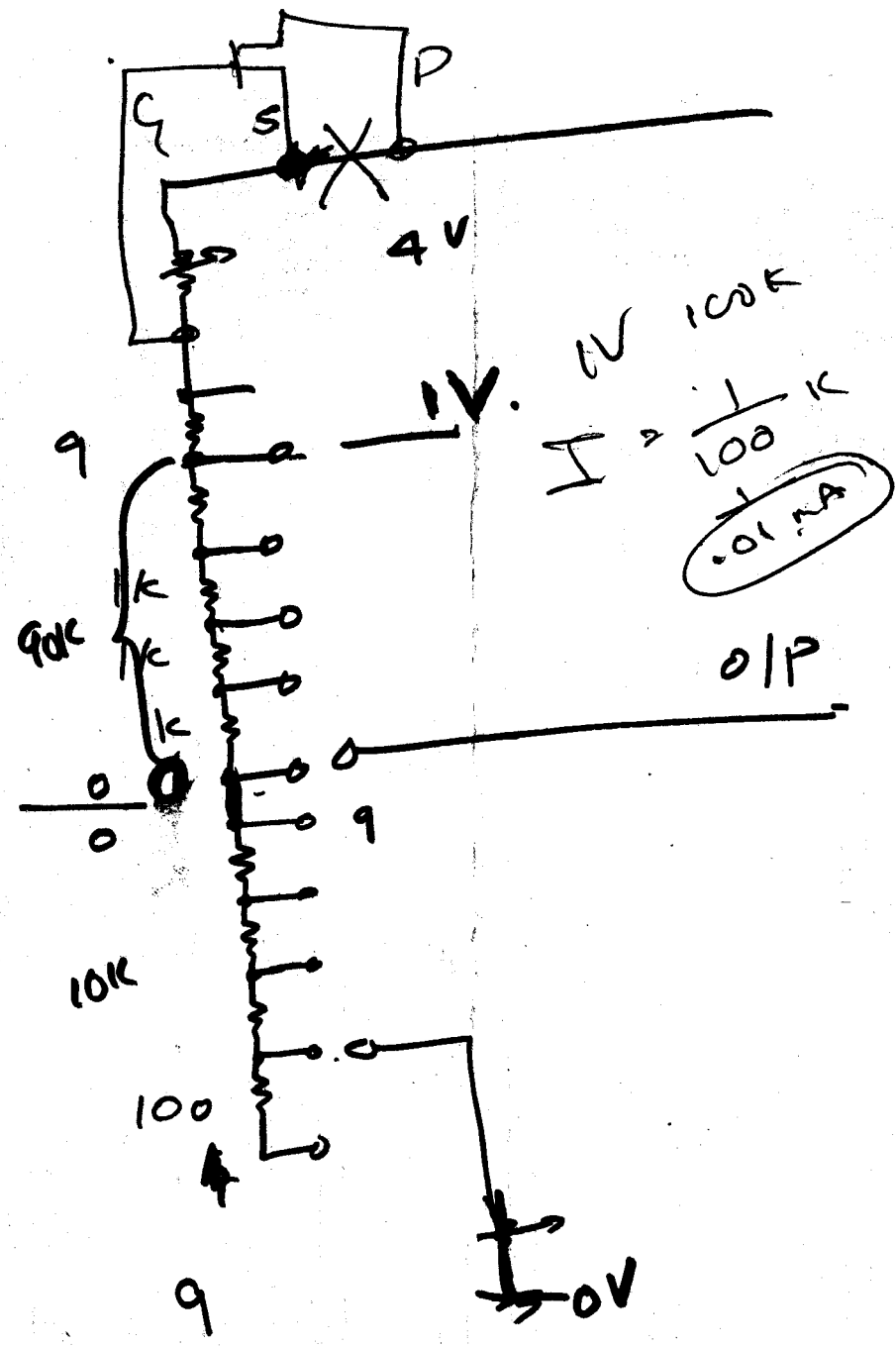
601
305
15.2

600k

590

2%

+ 1



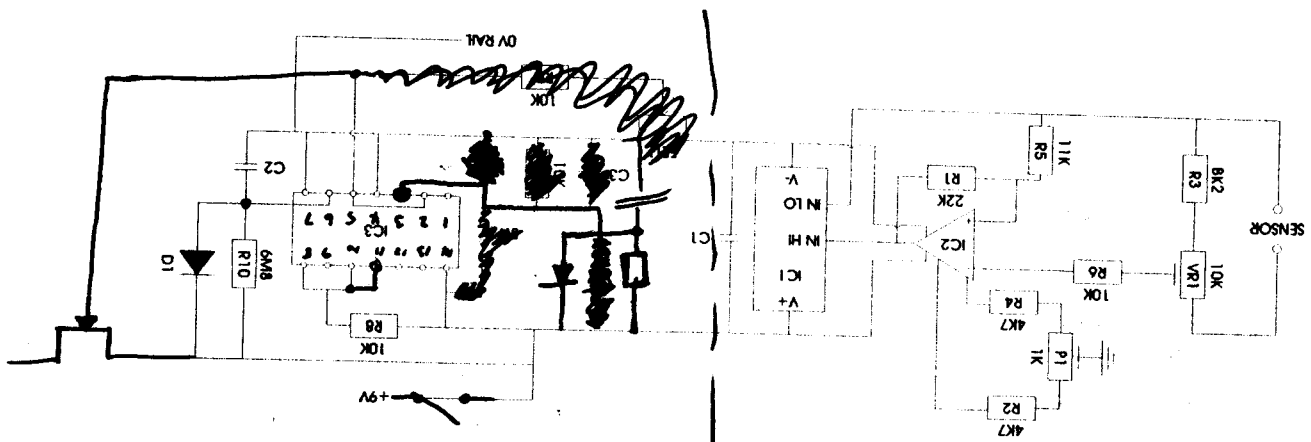
90k

99k
5V

10

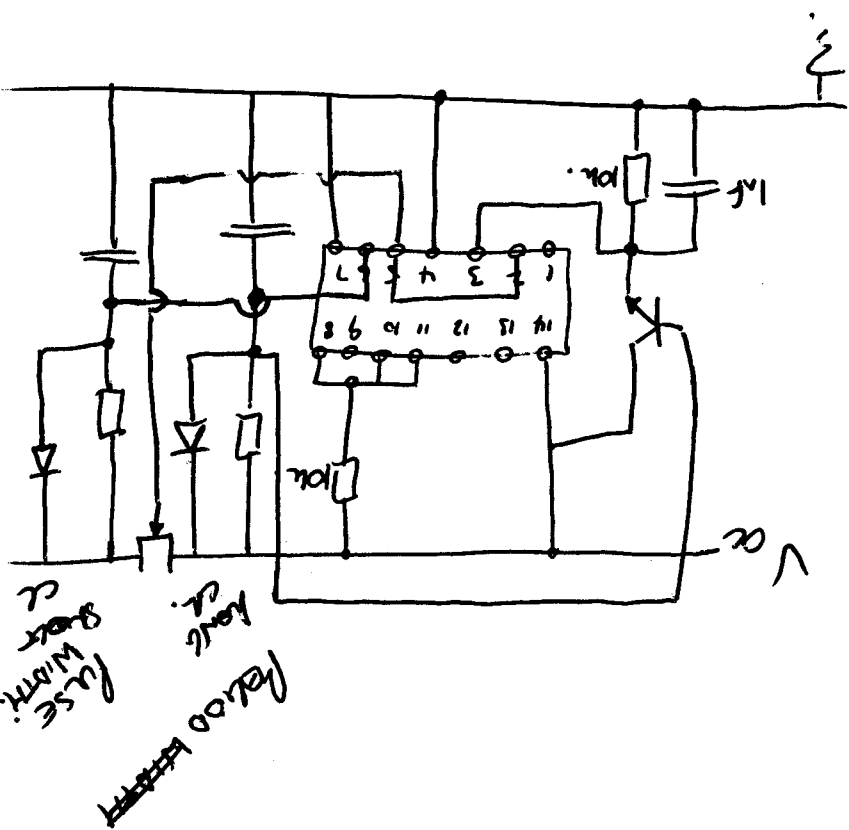
Circuit Design Considerations

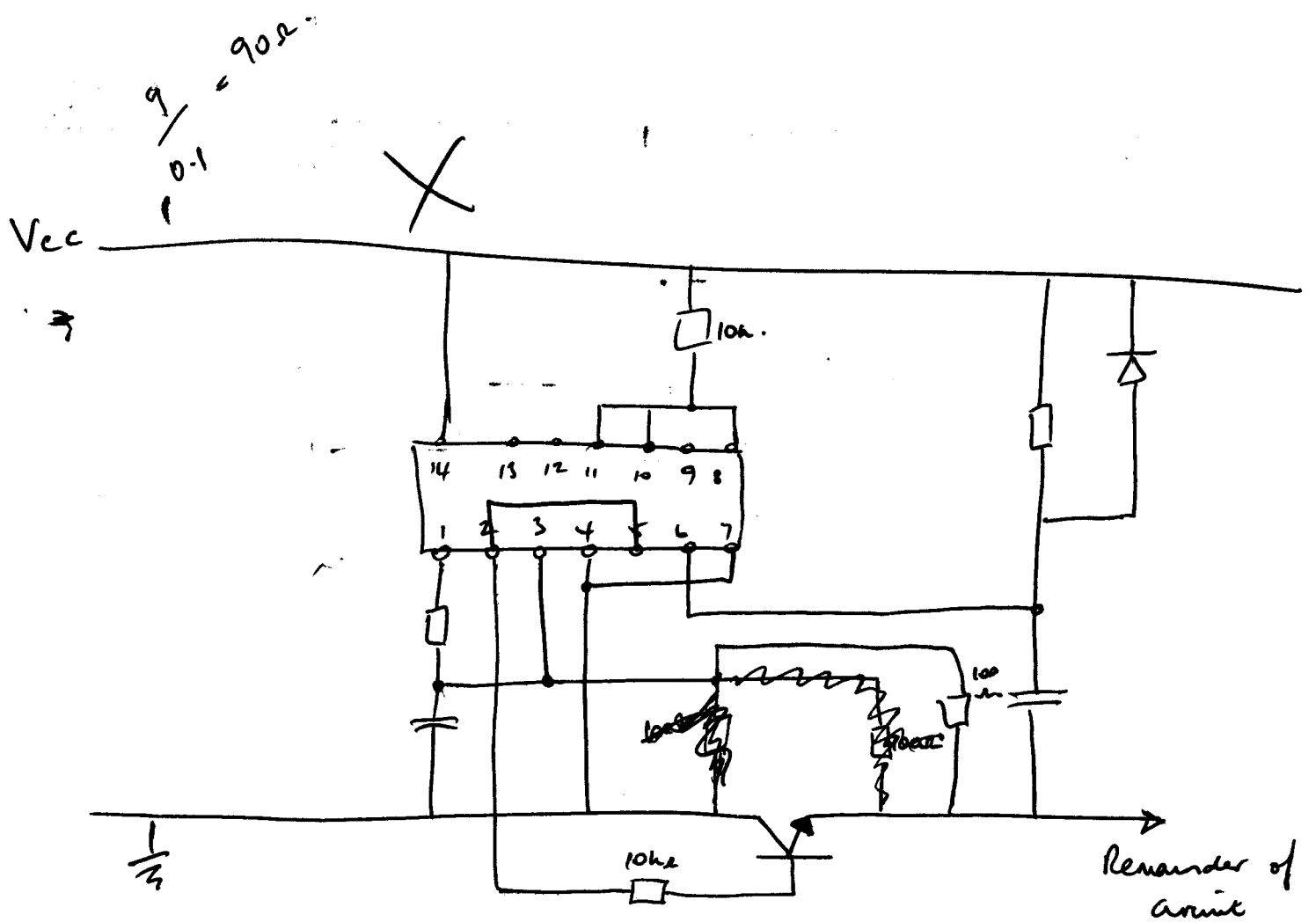
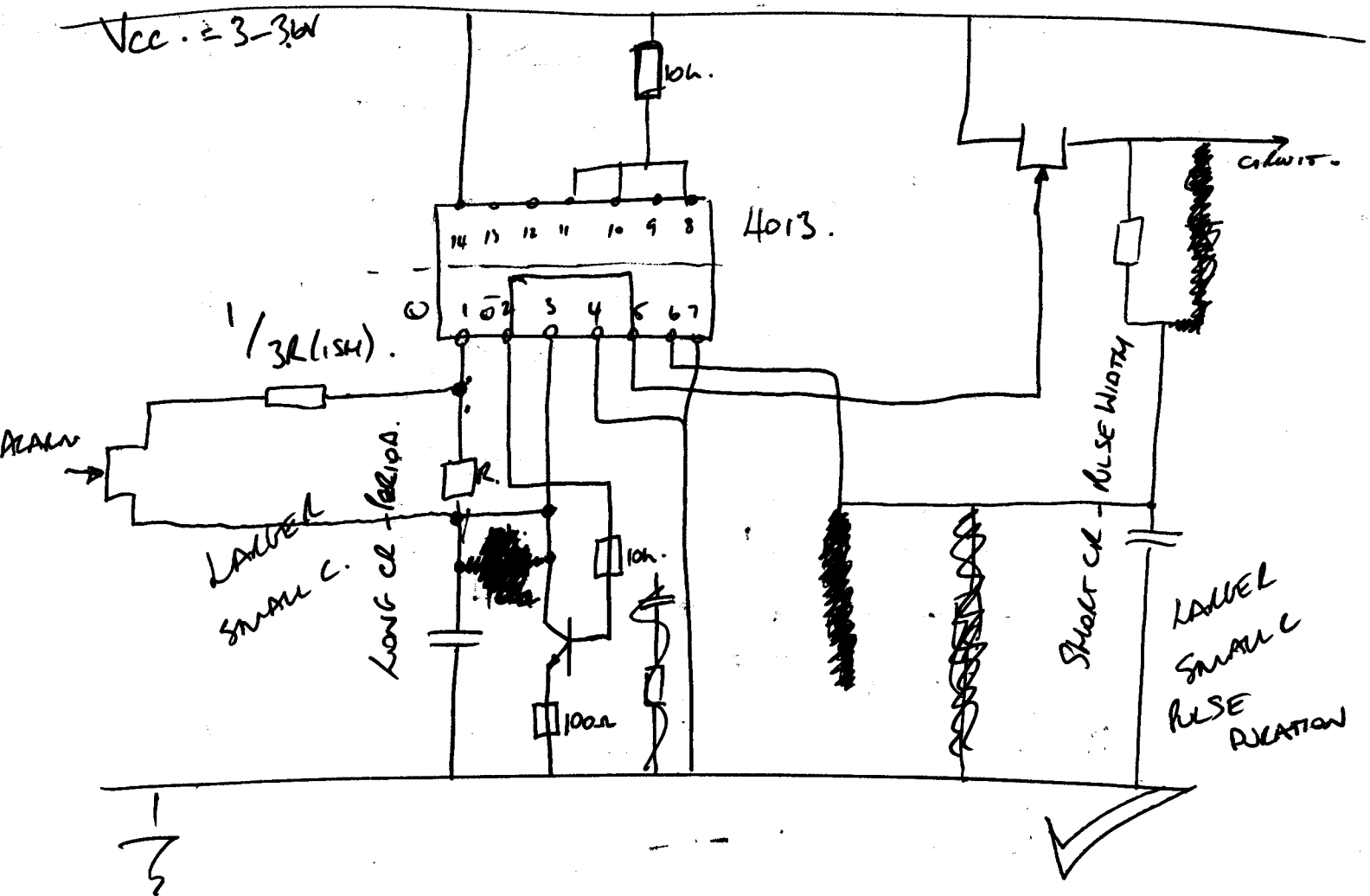
Circuit Schematic



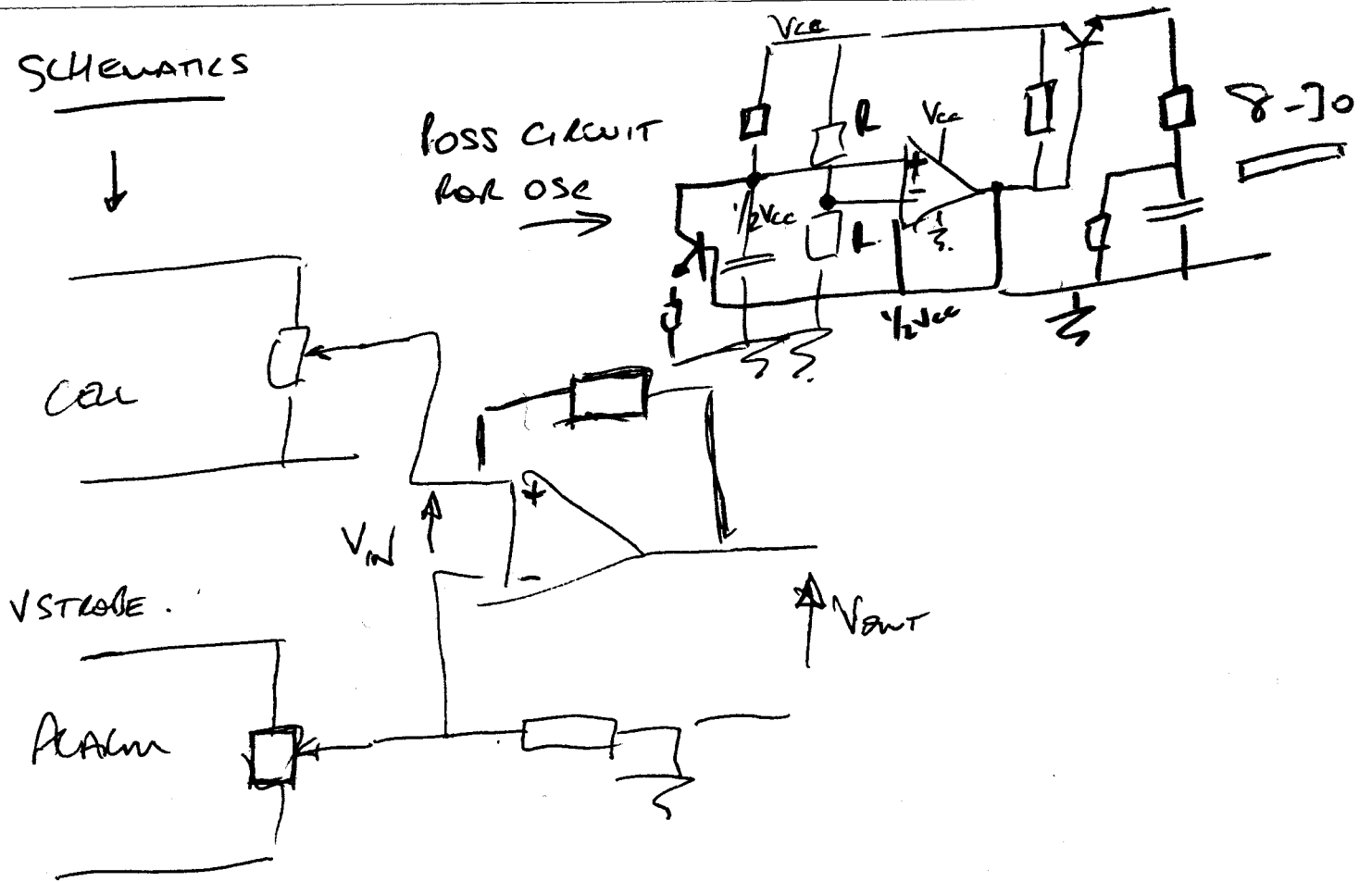
C1	10nF	IC1	DPM400
C2	33uF	IC2	TL071CP
C3	1nF	IC3	MC14013BCN
VR1	10K		
P1	1K Multi		
FET1	VN10KM		
D1	1N4148		

R1	22K
R2	4K7
R3	8K2
R4	4K7
R5	11K
R6	10K
R7	10K
R8	10K
R9	10K
R10	6M8
R11	10K





SCHEMATICS



~~1H~~. 57KS DURATION

Target : 43800 Ks. Cell cap 1AH.

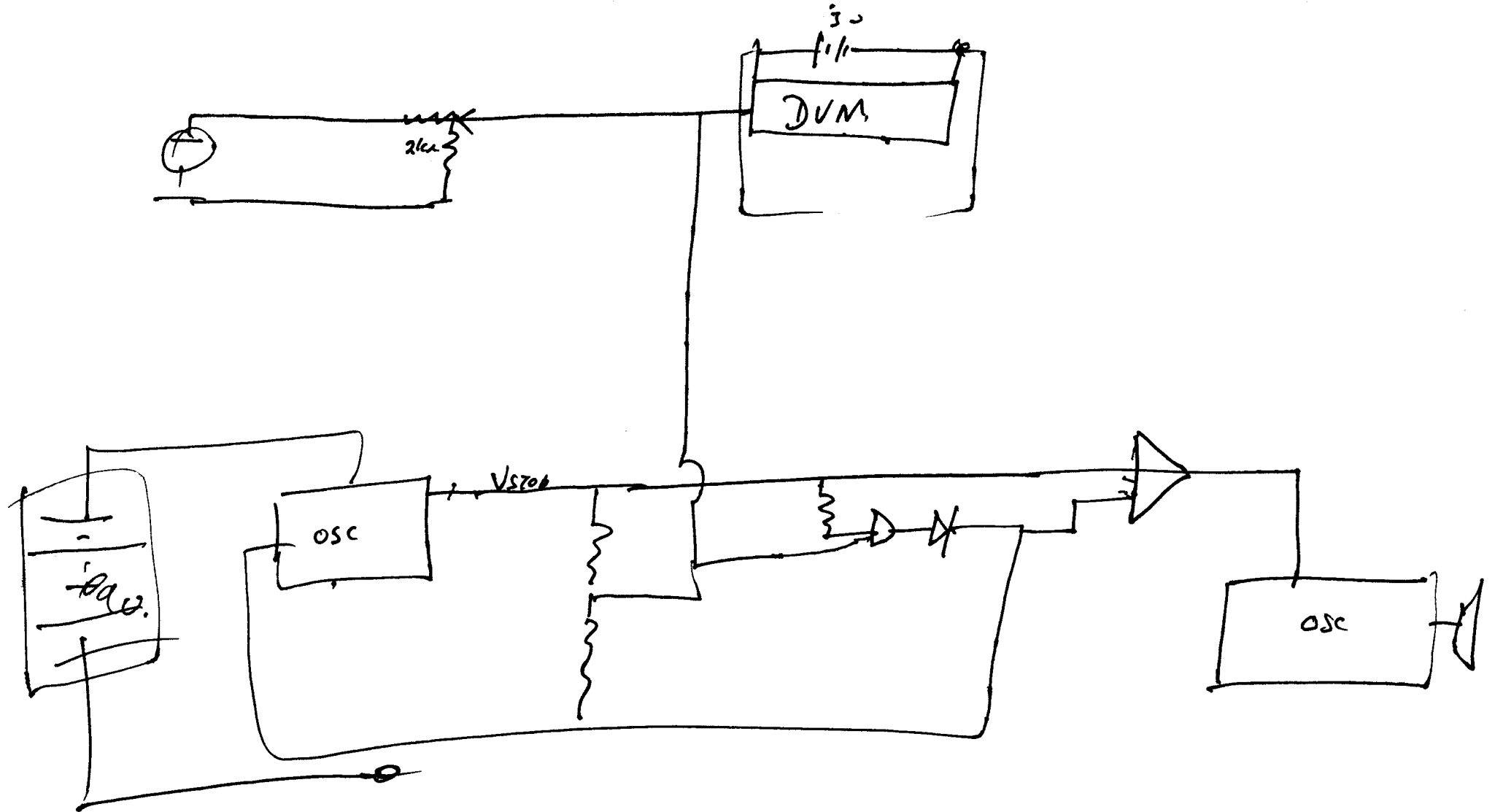
Target average current draw = 22.83 μ A.
 4.54 μ A @ 2.25 period / 50ms pulse + internal

3 1/3 μ A @ 3s period / 50ms pulse + internal

0.625 μ A @ 20s period / 50ms pulse + internal

2.38 Ω
 344 Ω

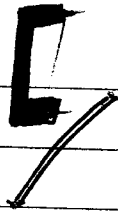
0.473 702 155
 1.473 702 155
 1.473 702 155



GL May 2000

INITIAL BRIEF

JANUARY

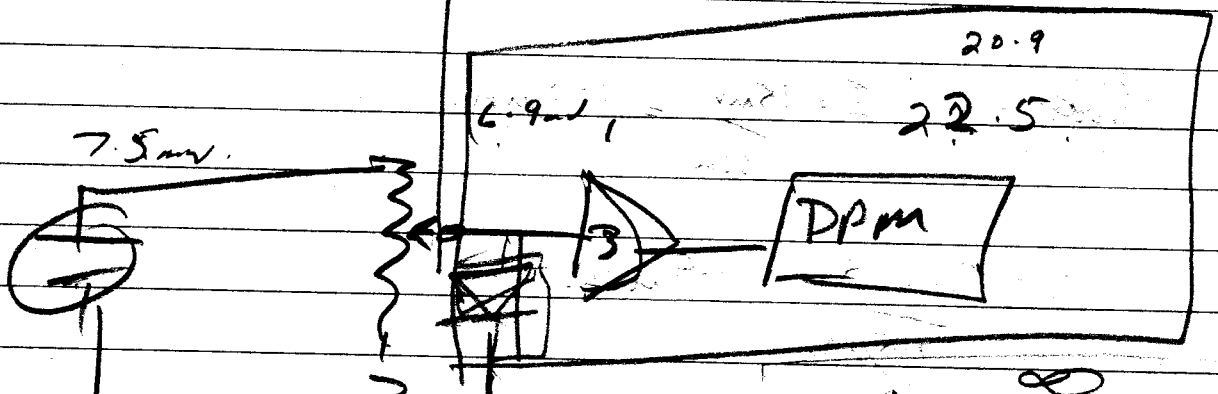


ask question
Possibility of
left or same diagram

AC 12V

10.5
10.

21%



7.5mv.

8.7
8.4
7.9
7.4

24
23
22

V_{out} C.F. Max

6.9v

mV CELL OUTPUT VOLTAGES.

202.9

6.4

19

5.9

18

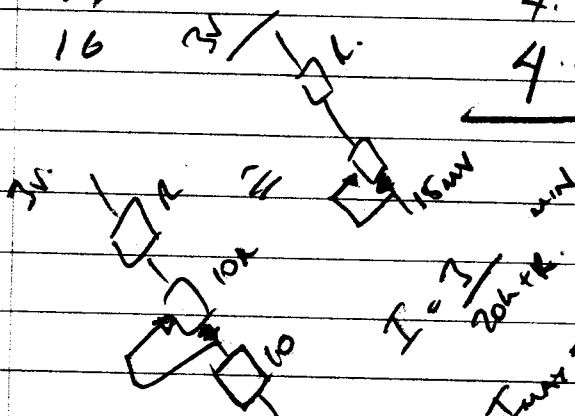
5.4

17

4.9

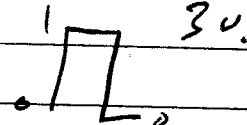
16

4.4



$$I = \frac{3}{20k + R}$$

$$I_{max} = \frac{3}{10k + R}$$



3v.

